ABSTRACT

0031 A method for forming a copper damascene feature including providing a semiconductor process wafer including at least one via opening formed to extend through a thickness of at least one dielectric insulating layer and an overlying trench line opening encompassing the at least one via opening to form a dual damascene opening; etching through an etch stop layer at the at least one via opening bottom portion to expose an underlying copper area; carrying out a sub-atmospheric DEGAS process with simultaneous heating of the process wafer in a hydrogen containing ambient; carrying out an in-situ sputter-clean process; and, forming a barrier layer in-situ to line the dual damascene opening.